REMARKS

The Applicant thanks the Examiner for the prompt and thorough final Office Action dated May 28, 2003.

The Examiner rejected claims 1 as being anticipated by the *Fornof* patent, U.S. Patent No. 6,537,908. The *Fornof* patent discloses a via first method for etching forming features in an interconnect structure or semiconductor device. *Fornof* discloses the use of a hard mask 54 including a stop layer 56 and a patterning layer 58, as shown in FIGs. 2B-2D, a via is etched in the mask layer 58, forming the opening 60. A trench is then patterned, which exposes the underlying dielectric 52, as shown in FIG. 2D.

With respect to amended independent claim 1, element (c) is amended as shown below:

> (c) then etching the mask layer to a second predetermined depth of the mask layer less than the first predetermined depth, forming a trench in the mask layer <u>without exposing the underlying dielectric material</u>.

Fornof cannot anticipate claim 1 because when the trench is etched to a second predetermined depth, the opening 62 exposes the underlying dielectric. In column 6, lines 19-22, Fornof explains, "Following the second etch which exposes the cured dielectric, the second photoresist is stripped from the structure utilizing conventional stripping process providing a structure such as shown in FIG. 2D. Column 6, lns 19-22.

The Examiner rejected independent claim 6 under 35 U.S.C. §103(a) as unpatentable over *Fornof* in view of the *Gutsche* reference. The *Gutsche* reference discloses a method of fabricating a semiconductor device that includes the formation of a mask layer having "*n*" mask films over three mask films. In FIGs. 1-2E, films 0, 1, 2, 3 of the mask layers are selectively etched to form a feature. The *Gutsche* reference discloses a single damascene method of fabrication as opposed to a dual damascene method of fabricating interconnect structures set forth in claim 1, 6 and 18. Accordingly,

Gutsche discloses a damascene material that etches only a single feature into the mask layer and transfers the feature to the underlying dielectric material.

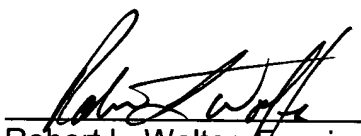
A combination of *Fornof* and *Gutsche* would, at most, discloses the use of a dual damascene process shown in *Fornof*, by which a via is first etched into a mask layer, and then a trench is subsequently etched, exposing the underlying dielectric material. Given the porosity of the low-k dielectric material, the photoresist will damage the low-k dielectric, which damage affects the integrity of the conductive lines and/or interconnections formed within the semiconductor device.

Accordingly, with respect to claim 6, neither *Fornof* nor *Gutsche* disclose all the elements of claim 6, nor would it have been obvious to combine *Fornof* and *Gutsche* to arrive at an invention having the limitations of claim 6. Claim 18 contains limitations similar to the amended claim 6, and is allowable for the above stated reasons.

Applicant respectfully requests reconsideration of claims 1-22, as amended.

If further prosecution of this application can be facilitated via telephone conference, the Examining Attorney is invited to contact the undersigned at (407) 926-7706.

Respectfully submitted,



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